Reg.No. \_\_\_\_\_\_\_\_\_\_\_\_



**UNIVERSITY**

(Karunya Institute of Technology & Sciences)

(Declared as Deemed-to-be University under Sec.3 of the UGC Act, 1956)

**End Semester Examination – Nov/Dec – 2016**

|  |  |  |  |
| --- | --- | --- | --- |
|  |  | **Semester :** | **2016-17 ODD** |
| **Code :** | **14EC3053** | **Duration :** | **3hrs** |
| **Sub. Name :** | **Design of Semiconductor Memories** | **Max. marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Q. No.** | **Sub Div.** | **Questions** | **Course**  **Outcome** | **Marks** |
| 1. | a. | With neat diagram explain the operation of a 3T and 1T DRAM cell. | CO2 | **16** |
| b. | Differentiate between hard error and soft error | CO1 | **4** |
| **(OR)** | | | | |
| 2. | a. | Justify the usage of trench capacitor in the design of high density DRAM. | CO1 | **4** |
| b. | With neat diagram explain the read, write operation of a conventional SRAM cell and the operation of its peripheral circuits (write circuitry and sense amplifier). | CO2 | **16** |
| 3. | a. | Justify the need for OTP EPROM | CO1 | **5** |
|  | b. | Indicate different memory cell design of PROM and explain how the cells are programmed. | CO3 | **15** |
| **(OR)** | | | | |
| 4. | a. | Justify that DRAM is used in Main memory. | CO1 | **5** |
|  | b. | Describe with necessary diagrams, different types of application specific SRAM. | CO1 | **15** |
| 5. | a. | Define Fowler-Nordheim tunneling mechanism with diagram. | CO1 | **5** |
|  | b. | With neat diagrams discuss about different EEPROM technologies and their impact on the performance of EEPROM. | CO3 | **15** |
| **(OR)** | | | | |
| 6. | a. | Explain how programming and reading is done in NAND structured cell EEPROM architecture. | CO2 | **16** |
|  | b. | List the differences between volatile and non-volatile memories with examples. | CO1 | **4** |
| 7. | a. | With state diagram, indicate how a 0 to 1 transition fault occur in a memory cell | CO2 | **5** |
|  | b. | Explain about IDDQ Fault modeling and Testing. | CO2 | **15** |
| **(OR)** | | | | |
| 8. | a. | Explain in detail about parametric testing in memories. | CO2 | **15** |
|  | b. | List three types of observable degradation effects upon exposing memories to ionizing radiation. | CO3 | **5** |
|  | | **Compulsory:** |  |  |
| 9. | a. | Mention the difference berween digital memories and analog memories. | CO2 | **4** |
|  | b. | With neat diagram of FRAM hysteresis curve explain the polarization effect, FRAM cell and memory operation. | CO2 | **16** |

ALL THE BEST